I Claim:

1. An integrated dynamic memory, comprising:

a memory cell array having a regular cell area with regular memory cells, a first test cell area with first test cells, and a second test cell area with second test cells, said regular memory cells, said first test cells and said second test cells being for storing a charge corresponding to an information bit;

a control unit for refreshing charge contents of said regular memory cells with a first refresh time;

a control unit for refreshing charge contents of said first test cells with a second refresh time, and for refreshing charge contents of said second test cells with a third refresh time; and

an evaluation unit for detecting memory cell defects in said first test cell area and in said second test cell area;

said first refresh time being shorter than said second refresh time; and

said second refresh time being shorter than said third refresh time.

2. The integrated dynamic memory according to claim 1, wherein: said evaluation unit includes a device for altering said first refresh time, said second refresh time, and said third refresh time based on said memory cell defects that were detected.

3. The integrated dynamic memory according to claim 1, wherein: said second refresh time is twice as long as said first refresh time, and said third refresh time is twice as long as said second refresh time.

4. The integrated dynamic memory according to claim 1, wherein:

said memory cell array is organized in row lines and column lines; and

said regular cell area includes a plurality of said row lines;

said first test cell area includes a plurality of said row lines; and

said second test cell area includes a plurality of said row lines.

5. The integrated dynamic memory according to claim 4, wherein:

said regular memory cell area has an edge; and

said plurality of said row lines of said first test cell area are configured next to one another at said edge of said regular memory cell area.

6. The integrated dynamic memory according to claim 4, wherein:

said regular memory cell area has an edge; and

said plurality of said row lines of said second test cell area are configured next to one another at said edge of said regular memory cell area.

7. The integrated dynamic memory according to claim 4, wherein:

said plurality of said row lines of said first test cell area are configured between said plurality of said row lines of said regular memory cell area.

8. The integrated dynamic memory according to claim 4, wherein:

said plurality of said row lines of said second test cell area are configured between said plurality of said row lines of said regular memory cell area.

9. A method for operating an integrated dynamic memory, which comprises:

providing the integrated dynamic memory with a memory cell array having a regular cell area with regular memory cells, a first test cell area with first test cells, and a second test cell area with second test cells;

providing the regular memory cells, the first test cells and the second test cells for storing a charge corresponding to an information bit;

refreshing charge contents of the regular memory cells with a first refresh time;

writing test patterns to the first test cells and to the second test cells;

refreshing charge contents of the first test cells with a second refresh time, and refreshing charge contents of the second test cells with a third refresh time;

providing the first refresh time being shorter than the second refresh time and providing the second refresh time being shorter than the third refresh time;

reading memory cell contents of the first test cell area and the second test cell area and detecting memory cell defects by comparing the memory cell contents with the test patterns that were written to the first test cells and to the second test cells; and

checking the first refresh time with regard to the memory cell defects that were detected in the first test cell area and in the second test cell area.

10. The method for operating an integrated dynamic memory according to claim 9, which comprises:

after the checking of the first refresh time:

if no memory cell defects are detected in the first test cell area and in the second test cell area and if a maximum refresh time has not been reached, then

lengthening the first refresh time, however, leaving the first refresh time unchanged after reaching the maximum refresh time;

if memory cell defects are detected in both the first test cell area and the second test cell area and if a minimum refresh time has not been reached, then shortening the first refresh time, however, leaving the first refresh time unchanged after reaching the minimum refresh time; and

otherwise leaving the first refresh time unchanged.

11. The method for operating an integrated dynamic memory according to claim 10, which comprises:

when the first refresh time is being lengthened, lengthening the second refresh time and the third refresh time so that the first refresh time is shorter than the second refresh time and the second refresh time is shorter than the third refresh time.

12. The method for operating an integrated dynamic memory according to claim 10, which comprises:

when the first refresh time is being shortened, shortening the second refresh time and the third refresh time so that the first refresh time is shorter than the second refresh time and the second refresh time is shorter than the third refresh time.

13. The method for operating an integrated dynamic memory according to claim 10, which comprises:

when the first refresh time is being lengthened, doubling the first refresh time, the second refresh time, and the third refresh time; and

when the first refresh time is being shortened, halving the first refresh time, the second refresh time, and the third refresh time.

14. The method for operating an integrated dynamic memory according to claim 9, wherein:

the first refresh time, the second refresh time, and the third refresh time each assume a value selected from a group consisting of 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, 1024 ms, 2048 ms, and 4096 ms.

15. The method for operating an integrated dynamic memory according to claim 9, which comprises:

performing a defect analysis when the memory cell defects are detected by ascertaining a type of the memory cell defects.

16. The method for operating an integrated dynamic memory according to claim 9, which comprises:

performing a defect analysis when the memory cell defects are detected by ascertaining a failure state selected from a group consisting of a failure of only logic zeros, a failure of only logic ones, and a failure of both logic ones and logic zeros.

17. A method for operating a plurality of integrated dynamic memories, which comprises:

providing each one of the plurality of the integrated dynamic memories with:

a memory cell array having a regular cell area with regular memory cells, a first test cell area with first test cells, and a second test cell area with second test cells, the regular memory cells, the first test cells and the second test cells being for storing a charge corresponding to an information bit;

a control unit for refreshing charge contents of the regular memory cells with a first refresh time;

a control unit for refreshing charge contents of the first test cells with a second refresh time, and for refreshing charge contents of the second test cells with a third refresh time; and

an evaluation unit for detecting memory cell defects in the first test cell area and in the second test cell area;

the first refresh time being shorter than the second refresh time; and

the second refresh time being shorter than the third refresh time;

for each one of the plurality of the integrated dynamic memories, in response to a request signal from an external controller, determining the first refresh time and communicating the first refresh time to the controller;

using the controller to determine a shortest refresh time selected from a group consisting of the first refresh time, the second refresh time, and the third refresh time; and

subsequently using the shortest refresh time for refreshing each one of the plurality of the integrated dynamic memories.

18. The method according to claim 17, which comprises:

for each one of the plurality of the integrated dynamic memories, continuously determining the second refresh time and the third refresh time and storing the second refresh time and the third refresh time in registers;

using the controller to read out the second refresh time and the third refresh time of all of the plurality of the integrated dynamic memories; and

using the controller to, based on the second refresh time and the third refresh time of all of the plurality of the integrated dynamic memories, decide whether to output a request signal for determining the first refresh time of each one of the plurality of the integrated dynamic memories.

19. The method according to claim 18, which comprises:

configuring the plurality of the integrated dynamic memories on a common substrate to form a module.

20. The method according to claim 18, which comprises:

configuring the plurality of the integrated dynamic memories on a common substrate to form a module.